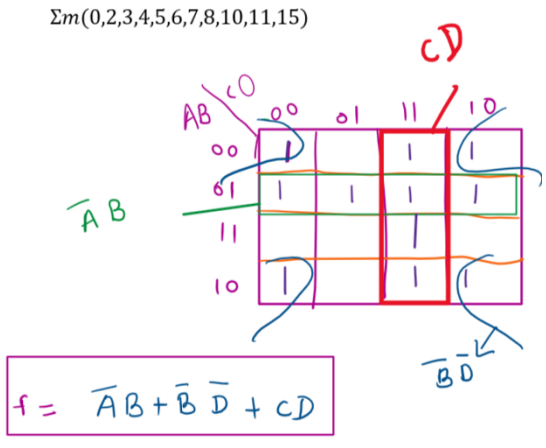
(Affiliated to University of Mumbai)	***End Semester Examination (R-24)FH 2026*** ***Answer Key with marking scheme***
Branch: ALL	Course: Digital System Design
Year/ Semester: FE/II	Course code:FEC204
Time: 03 hours	Marks: 80

		Marks
Q. 1	Attempt any FOUR. (All questions carry equal marks)	
A.	Integer Part (76): 1. Divide by 2, noting the remainders: Now, reading the remainders from bottom to top: $76_{10} = 1001100_2$--------2 Marks Fractional Part (0.22): 1. Multiply by 2, noting the integer parts: $0.22_{10} \approx 0.001110_2$ ----------2 Marks Result:$(76.22)_{10} = 1001100.001110_2$ ----------1 Mark	05
B.	Encoder block diagram --------- 1 Mark Truth table ---------- 1 Mark Expression ---------- 2 Marks logic diagram. --------- 1 Mark	05
C.	Compare Mealy and Moore Machine including diagram ---------Answer with 5 detailed points.--- 5 Marks	05
D.	AB'+BC+AC+A'C = AB'(C+C')+(A+A')BC+A(B+B')C+A'(B+B')C------2 Marks =AB'C+AB'C'+ABC+A'BC+ABC+AB'C+A'BC+A'B'C-----1Mark =AB'C+AB'C'+ABC+A'BC+A'BC+A'B'C --------- 2 Marks	05
E.	Excitation table, ---- 1 Mark conversion table ---- 2 Marks K Map and expression ---1 Mark logic diagram.----1 Mark	05
F.	SRAM and DRAM.------- -Answer with 5 detailed points.--- 5 Marks	05
Q.2	Attempt any FOUR. (All questions carry equal marks)	
A.	45 ---101101 ----- 1 Mark 55-----110111---- 1 Mark 1 's complement method with justification ----4 Marks 2's complement method with justification ------ 4 marks	10
B.	X –OR gate using NAND gate Diagram ---1 Mark Final Boolean Expression from diagram --- 1 Mark Simplification and Justification ---- 3 Marks X –NOR gate using NAND gate Diagram ---1 Mark Final Boolean Expression from diagram --- 1 Mark	10

	Simplification and Justification ---- 3 Marks	
C.	2 –bit comparator truth table ----2 Marks K map ---- 3 Marks Expression --- 3 Marks logic diagram using gates.---- 2 Marks	10
D.	SR Flip Flop with logic diagram ------- 2 Marks Justify operation/working with different input conditions.---- 4 Marks Truth table ---2 Marks Excitation Table ----2 Marks	10
E.	i) Full adder with help of truth table ---- 2 Mark K – Map and expressions---- 2 Marks and the logic diagram--- 1 Mark	05
	ii) Full adder using 4:1 multiplexer with help of truth table ------- 3 marks logic diagram ---2 Marks	05
F.	synchronous 3 bit up-down counter using JK Flip Flop flip flop excitation table---1 Mark state diagram ----1 Mark counter table 3 Marks K map and expression --- 3 Marks logic diagram----2 Marks	10
Q.3	Attempt any FOUR. (All questions carry equal marks)	
A.	State and explain Demorgan's theorem. --- 3 Marks Verify using truth table. 2 Marks	05
B.	K map ---2 Marks Conversion and implementation using NAND gate --- 3Marks 	05

C.	Compare Synchronous and Asynchronous counter. ---Answer with 5 detailed points.---- 5 Marks	05
D.	FSM table (Present state, next state, output, T_A , T_B)--- 2 Marks K map and expression --- 2 Mark Design ---1 Mark	05
E.	Design 3 bit Binary to Gray code converter Truth table – 1 mark K map and Expression -----2 Marks logic diagram using PLA.----2 Marks	05
F.	Explain with help of diagram working of Serial In Serial out Shift register. Diagram ---2 Marks Explanation ---3 Marks	05